

UNITED STATES PATENT AND TRADEMARK OFFICE

**CERTIFICATE OF CORRECTION**

Pg 1026

PATENT NO. : 7,071,557 B2  
APPLICATION NO. : 09/388,031  
DATED : July 4, 2006  
INVENTOR(S) : Salman Akram

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

The drawing sheets, consisting of Figs. 3a, 3b and 5, should be deleted to be replaced with the drawing sheets, consisting of Figs. 3a, 3b and 5, as shown on the attached pages.



US007071557B2

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(12) **United States Patent**  
**Akram**

(10) **Patent No.:** **US 7,071,557 B2**  
(45) **Date of Patent:** **\*Jul. 4, 2006**

(54) **METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME**

(75) **Inventor:** **Salman Akram, Boise, ID (US)**

(73) **Assignee:** **Micron Technology, Inc., Boise, ID (US)**

(\*) **Notice:** This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154 (a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/388,031**

(22) **Filed:** **Sep. 1, 1999**

(65) **Prior Publication Data**

US 2002/0056914 A1 May 16, 2002

(51) **Int. Cl.**  
**H01L 23/52 (2006.01)**

(52) **U.S. Cl.** ..... **257/751; 257/748; 257/773; 257/774; 257/762; 257/758**

(58) **Field of Classification Search** ..... **257/301, 257/296, 669, 750, 752, 486, 751, 748, 741, 257/773, 774, 762, 758; 438/625, 627, 643, 438/653**

See application file for complete search history.

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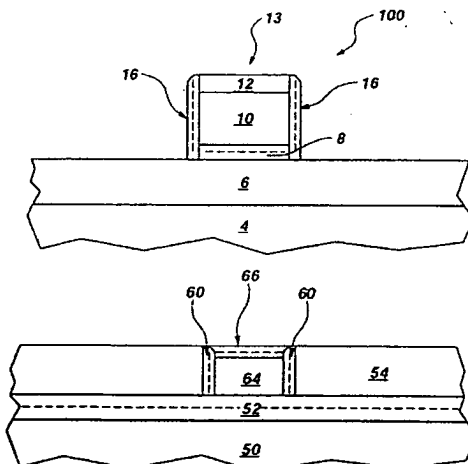
*Primary Examiner*—Eugene Lee

(74) *Attorney, Agent, or Firm*—TraskBritt

(57) **ABSTRACT**

The present invention provides a metallization structure for semiconductor device interconnects such as a conductive line, and methods for making the same, wherein the metallization structure includes a substrate with a substantially planar upper surface, a foundation metal layer disposed on a portion of the substrate upper surface, a primary conducting metal layer overlying the foundation metal layer, and a metal spacer on the sidewalls of the primary conducting metal layer and the foundation metal layer. The present invention also provides a metallization structure and a method for making the same, wherein the metallization structure includes a substrate with a foundation metal layer disposed thereon, a dielectric layer with an aperture there-through being disposed on the substrate, where the bottom of the aperture exposes the foundation metal layer of the substrate and a metal spacer on the sidewall of the aperture and a line or plug of a primary conducting metal filling the remaining portion of the aperture. These metallization structures are useful for reducing the incidence and severity of thermally induced stress voids.

**52 Claims, 9 Drawing Sheets**



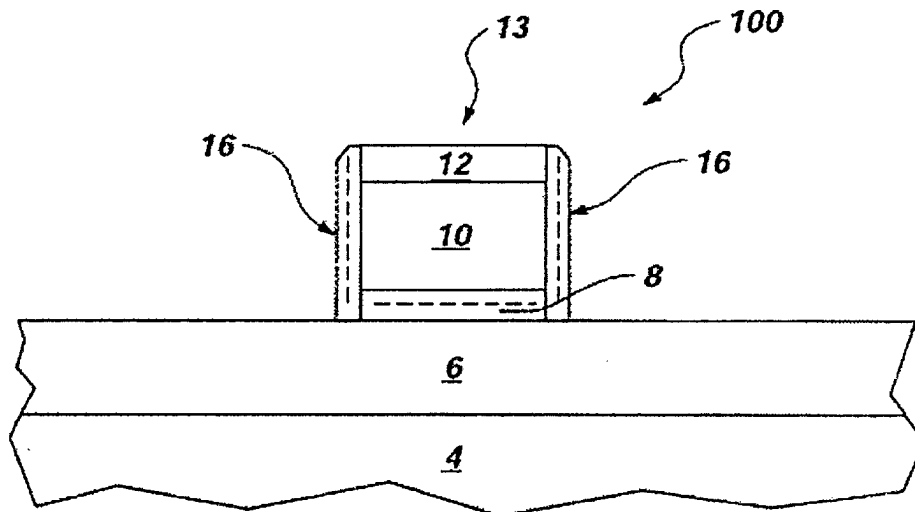
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:



**Fig. 3a**

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell  
TRASKBRITT  
230 South 500 East, Suite 300  
Salt Lake City, Utah 84102 USA

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.  
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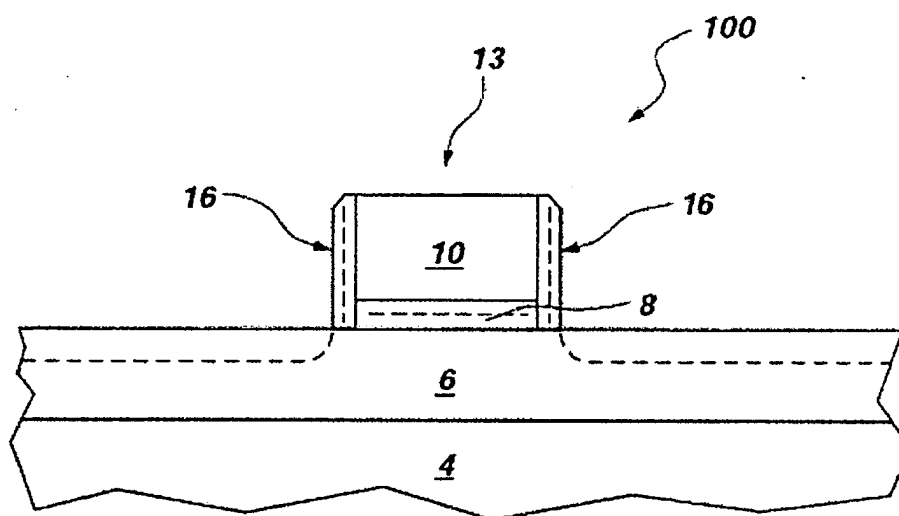
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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:



**Fig. 3b**

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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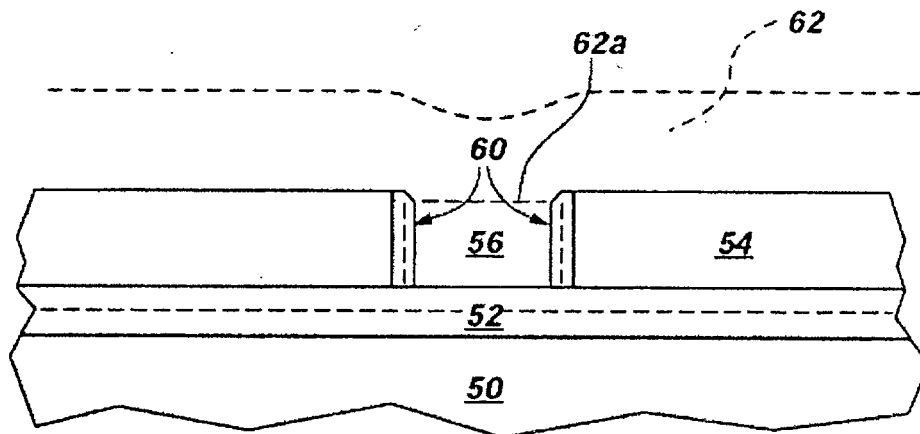


Fig. 5

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 7, LINE 52, change "for sec ond" to --for second--

CLAIM 45, COLUMN 12, LINE 47, change "The structure of claim 41," to --The structure of claim 44,--

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